50 MHz to 9 GHz 65 dB TruPwr Detector

ADL5902

FEATURES

- Accurate rms-to-dc conversion from 50 MHz to 9 GHz
- Single-ended input dynamic range of 65 dB
  - No balun or external input matching required
- Waveform and modulation independent, such as
  - GSM/CDMA/W-CDMA/TD-SCDMA/WiMAX/LTE
- Linear-in-decibels output, scaled 53 mV/dB
- Transfer function ripple: <±0.1 dB
- Temperature stability: <±0.3 dB
- All functions temperature and supply stable
- Operates from 4.5 V to 5.5 V from −40°C to +125°C
- Power-down capability to 1.5 mW
- Pin-compatible with the 50 dB dynamic range AD8363

APPLICATIONS

- Power amplifier linearization/control loops
- Transmitter power controls
- Transmitter signal strength indication (TSSI)
- RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

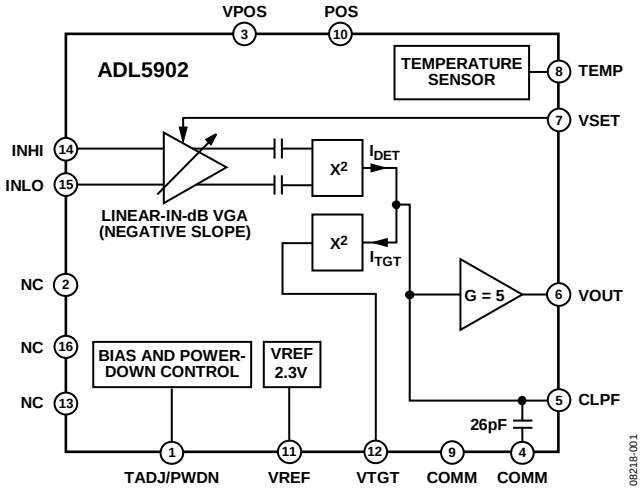

Figure 1.

GENERAL DESCRIPTION

The ADL5902 is a true rms responding power detector that has a 65 dB measurement range when driven with a single-ended 50 Ω source. This feature makes the ADL5902 frequency versatile by eliminating the need for a balun or any other form of external input tuning for operation up to 9 GHz.

The ADL5902 provides a solution in a variety of high frequency systems requiring an accurate measurement of signal power. Requiring only a single supply of 5 V and a few capacitors, it is easy to use and capable of being driven single-ended or with a balun for differential input drive. The ADL5902 can operate from 50 MHz to 9 GHz and can accept inputs from −62 dBm to at least +3 dBm with large crest factors, such as GSM, CDMA, W-CDMA, TD-SCDMA, WiMAX, and LTE modulated signals.

The ADL5902 can determine the true power of a high frequency signal having a complex low frequency modulation envelope or can be used as a simple low frequency rms voltmeter. Used as a power measurement device, VOUT is connected to VSET. The output is then proportional to the logarithm of the rms value of the input. In other words, the reading is presented directly in decibels and is scaled 1.06 V per decade, or 53 mV/dB; other slopes are easily arranged. In controller mode, the voltage applied to VSET determines the power level required at the input to null the deviation from the set point. The output buffer can provide high load currents.

The ADL5902 has 1.5 mW power consumption when powered down by a logic high applied to the PWDN pin. It powers up within approximately 5 µs to its nominal operating current of 73 mA at 25°C. The ADL5902 is supplied in a 4 mm × 4 mm, 16-lead LFCSP for operation over the wide temperature range of −40°C to +125°C.

The ADL5902 is also pin-compatible with the AD8363, 50 dB dynamic range TruPwr™ detector. This feature allows the designer to create one circuit layout for projects requiring different dynamic ranges. A fully populated RoHS-compliant evaluation board is available.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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REVISION HISTORY

4/10—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, single-ended input drive, R_T = 60.4 Ω, VOUT connected to VSET, V_{TGT} = 0.8 V, C_{LPF} = 0.1 µF. Negative current values imply that the ADL5902 is sourcing current out of the indicated pin.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			50 to 9000		MHz
RF INPUT INTERFACE	Pins INHI, INLO, ac-coupled				
Input Impedance	Single-ended drive, 50 MHz		2000		Ω
Common Mode Voltage			2.5		V
100 MHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.5 V		63		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.11/+0.25		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.22/+0.15		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		−0.35/+0.25		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		−0.22/+0.15		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		53.8		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.1		dBm
700 MHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C,V_{TADJ} = 0.4 V		61		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		+0.3/−0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.1/0		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		+0.3/−0.4		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		−0.1/0		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		53.7		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.8		dBm
900 MHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.4 V		61		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		+0.3/−0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		0/−0.1		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		+0.3/−0.4		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		0/−0.1		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		53.7		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.7		dBm

Parameter	Test Conditions	Min	Typ	Max	Unit
Deviation from CW Response	11.02 dB peak-to-rms ratio (CDMA2000)		−0.1		dB
	5.13 dB peak-to-rms ratio (16 QAM)		−0.05		dB
	2.76 dB peak-to-rms ratio (QPSK)		−0.05		dB
1.9 GHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.4 V		64		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		−61		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.1/0		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.3/+0.3		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		−0.1/0		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		−0.3/+0.4		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm, and 0 dBm		52.6		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.6		dBm
2.14 GHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.4 V		65		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −45 dBm, and 0 dBm		−62		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.1/0		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.3/+0.3		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		−0.1/0		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		−0.3/+0.4		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		52.4		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.9		dBm
Deviation from CW Response	12.16 dB peak-to-rms ratio (four-carrier W-CDMA)		−0.1		dB
	11.58 dB peak-to-rms ratio (LTE TM1 1CR 20 MHz BW)		−0.1		dB
	10.56 dB peak-to-rms ratio (one-carrier W-CDMA)		−0.1		dB
	6.2 dB peak-to-rms ratio (64 QAM)		−0.07		dB
2.6 GHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.45 V		65		dB
Maximum Input Level, ±1.0 dB	Calibration at −60, −45 and 0 dBm		5		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60, −45 and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		0.4/0		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		+0.5/−0.6		dB
	−40°C < T_A < +125°C; P_{IN} = 0 dBm		0.6/0		dB
	−40°C < T_A < +125°C; P_{IN} = −45 dBm		+0.7/−0.6		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		51.0		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −45 dBm and 0 dBm		−62.1		dBm
3.5 GHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.5 V		57		dB
Maximum Input Level, ±1.0 dB	Calibration at −60 dBm, −40 dBm, and 0 dBm		8		dBm
Minimum Input Level, ±1.0 dB	Calibration at −60 dBm, −40 dBm, and 0 dBm		−49		dBm

Parameter	Test Conditions	Min	Typ	Max	Unit
Deviation vs. Temperature	Deviation from output at 25°C				
	$-40°C < T_A < +85°C$; P_{IN} = 0 dBm		0.2/0		dB
	$-40°C < T_A < +85°C$; P_{IN} = −40 dBm		−0.2/+0.4		dB
	$-40°C < T_A < +125°C$; P_{IN} = 0 dBm		+0.2/−0.3		dB
	$-40°C < T_A < +125°C$; P_{IN} = −40 dBm		−0.2/+0.4		dB
Logarithmic Slope	−40 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and 0 dBm		49.6		mV/dB
Logarithmic Intercept	−40 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and 0 dBm		−63.1		dBm
5.8 GHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C, V_{TADJ} = 0.95 V		61		dB
Maximum Input Level, ±1.0 dB	Calibration at −50 dBm, −30 dBm, and 0 dBm		9		dBm
Minimum Input Level, ±1.0 dB	Calibration at −50 dBm, −30 dBm, and 0 dBm		−52		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	$-40°C < T_A < +85°C$; P_{IN} = 0 dBm		−0.8/0		dB
	$-40°C < T_A < +85°C$; P_{IN} = −30 dBm		−1.3/+0.1		dB
	$-40°C < T_A < +125°C$; P_{IN} = 0 dBm		−1.6/0		dB
	$-40°C < T_A < +125°C$; P_{IN} = −30 dBm		−1.3/+0.1		dB
Logarithmic Slope	−30 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and 0 dBm		42.7		mV/dB
Logarithmic Intercept	−30 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and 0 dBm		−54.1		dBm
OUTPUT INTERFACE	VOUT (Pin 6)				
Output Swing, Controller Mode	Swing range minimum, R_L ≥ 500 Ω to ground		0.03		V
	Swing range maximum, R_L ≥ 500 Ω to ground		4.8		V
Current Source/Sink Capability				10/10	mA
Voltage Regulation	I_{LOAD} = 8 mA, source/sink		+0.2/−0.2		%
Output Noise	RF_{IN} = 2.14 GHz, −20 dBm, f_{NOISE} = 100 kHz, C_{LPF} = 220 pF		25		nV/√Hz
Rise Time	Transition from no input to 1 dB settling at P_{IN} = −10 dBm, C_{LPF} = 220 pF		3		µs
Fall Time	Transition from −10 dBm to off (1 dB of final value), C_{LPF} = 220 pF		25		µs
SETPOINT INPUT	VSET (Pin 7)				
Voltage Range	Log conformance error ≤ 1 dB, minimum 2.14 GHz		3.5		V
	Log conformance error ≤ 1 dB, maximum 2.14 GHz		0.23		V
Input Resistance			72		kΩ
Logarithmic Scale Factor	f = 2.14 GHz		52.4		mV/dB
Logarithmic Intercept	f = 2.14 GHz		−62.9		dBm
TEMPERATURE COMPENSATION	Pin TADJ/PWDN (Pin 1)				
Input Voltage Range		0		V_S	V
Input Bias Current	V_{TADJ} = 0.4 V		2		µA
Input Resistance	V_{TADJ} = 0.4 V		200		kΩ
VOLTAGE REFERENCE	VREF (Pin 11)				
Output Voltage	P_{IN} = −55 dBm		2.3		V
Temperature Sensitivity	25°C ≤ T_A ≤ 125°C		−0.16		mV/°C
	−15°C ≤ T_A ≤ +25°C		0.045		mV/°C
	−40°C ≤ T_A ≤ −15°C		−0.04		mV/°C
Short-Circuit Current Source/ Sink Capability	25°C ≤ T_A ≤ 125°C		4/0.05		mA
	−40°C ≤ T_A < +25°C		3/0.05		mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 2 mA		−0.4		%

Parameter	Test Conditions	Min	Typ	Max	Unit
TEMPERATURE REFERENCE	TEMP (Pin 8)				
Output Voltage	T_A = 25°C, $R_L \geq$ 10 kΩ		1.4		V
Temperature Coefficient	−40°C ≤ T_A ≤ +125°C, $R_L \geq$ 10 kΩ		4.9		mV/°C
Short-Circuit Current Source/ Sink Capability	25°C ≤ T_A ≤ 125°C		4/0.05		mA
	−40°C ≤ T_A < +25°C		3/0.05		mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 1 mA		−2.8		%
RMS TARGET INTERFACE	VTGT (Pin 12)				
Input Voltage Range		0.2		2.5	V
Input Bias Current	V_{TGT} = 0.8 V		8		µA
Input Resistance			100		kΩ
POWER-DOWN INTERFACE	Pin TADJ/PWDN (Pin 1)				
Voltage Level to Enable	V_{PWDN} decreasing			4	V
Voltage Level to Disable	V_{PWDN} increasing	4.9			V
Input Current	V_{PWDN} = 5 V		1		µA
	V_{PWDN} = 4.5 V		500		µA
	V_{PWDN} = 0 V		3		µA
Enable Time	V_{TADJ} low to V_{OUT} at 1 dB of final value, $C_{LPA/B}$ = 220 pF, P_{IN} = 0 dBm		5		µs
Disable Time	V_{TADJ} high to V_{OUT} at 1 dB of final value, $C_{LPA/B}$ = 220 pF, P_{IN} = 0 dBm		3		µs
POWER SUPPLY INTERFACE	VPOS (Pin 3, Pin 10)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	T_A = 25°C, P_{IN} < −60 dBm		73		mA
	T_A = 125°C, P_{IN} < −60 dBm		90		mA
Power-Down Current	$V_{TADJ} > V_S$ − 0.1 V		300		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Average RF Power[1]	21 dBm
Equivalent Voltage, Sine Wave Input	2.51 V p-p
Internal Power Dissipation	550 mW
θ_{JC}[2]	10.6°C/W
θ_{JB}[2]	35.3°C/W
θ_{JA}[2]	57.2°C/W
Ψ_{JT}[2]	1.0°C/W
Ψ_{JB}[2]	34°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] This is for long durations. Excursions above this level, with durations much less than 1 second, are possible without damage.
[2] No airflow with the exposed pad soldered to a 4-layer JEDEC board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

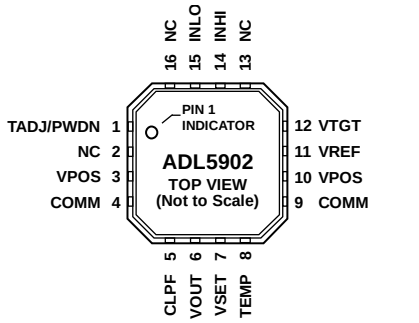

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TADJ/PWDN	This is a dual function pin used for controlling the amount of nonlinear intercept temperature compensation at voltages <2.5 V and/or for shutting down the device at voltages >4 V. If the shutdown function is not used, this pin can be connected to the VREF pin through a voltage divider. See Figure 41 for an equivalent circuit.
2	NC	No Connect.
3, 10	VPOS	Supply for the Device. Connect this pin to a 5 V power supply. Pin 3 and Pin 10 are not internally connected; therefore, both must connect to the source.
4, 9, EPAD	COMM	System Common Connection. Connect these pins via low impedance to system common. The exposed paddle is also COMM and should have both a good thermal and good electrical connection to ground.
5	CLPF	Connection for RMS Averaging Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to modify loop stability and response time. See Figure 43 for an equivalent circuit.
6	VOUT	Output. In measurement mode, this pin is connected to VSET. In controller mode, this pin can be used to drive a gain control element. See Figure 43 for an equivalent circuit.
7	VSET	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current flow in the loop integrating capacitor pin, CLPF. This pin controls the variable gain amplifier (VGA) gain such that a 50 mV change in V_{SET} changes the gain by approximately 1 dB. See Figure 42 for an equivalent circuit.
8	TEMP	Temperature Sensor Output of 1.4 V at 25°C with a Coefficient of 5 mV/°C. See Figure 38 for an equivalent circuit.
11	VREF	General-Purpose Reference Voltage Output of 2.3 V at 25°C. See Figure 39 for an equivalent circuit.
12	VTGT	The voltage applied to this pin determines the target power at the input of the RF squaring circuit. The intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity; however, this may affect the system loop response. See Figure 44 for an equivalent circuit.
13	NC	No Connect.
14	INHI	RF Input. The RF input signal is normally ac-coupled to this pin through a coupling capacitor. See Figure 37 for an equivalent circuit.
15	INLO	RF Input Common. This pin is normally ac-coupled to ground through a coupling capacitor. See Figure 37 for an equivalent circuit.
16	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, Z_O = 50 Ω, single-ended input drive, VOUT connected to VSET, V_{TGT} = 0.8 V, C_{LPF} = 0.1 µF, T_A = +25°C (black), −40°C (blue), +85°C (red), +125°C (orange) where appropriate. Error referred to the best fit line (linear regression) from − 10 dBm to − 40 dBm, unless otherwise indicated. Input RF signal is a sine wave (CW), unless otherwise indicated.

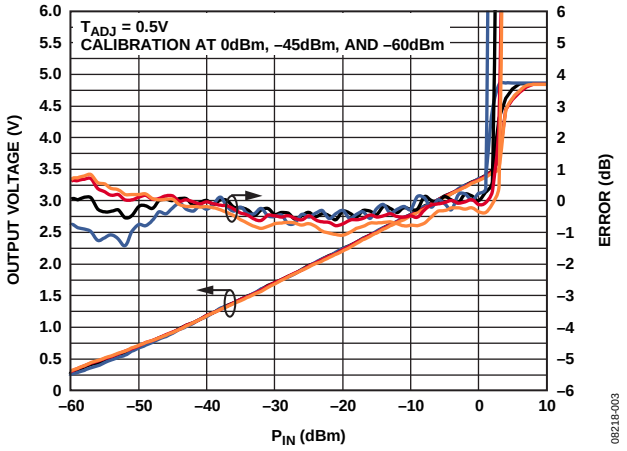

Figure 3. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 100 MHz, CW

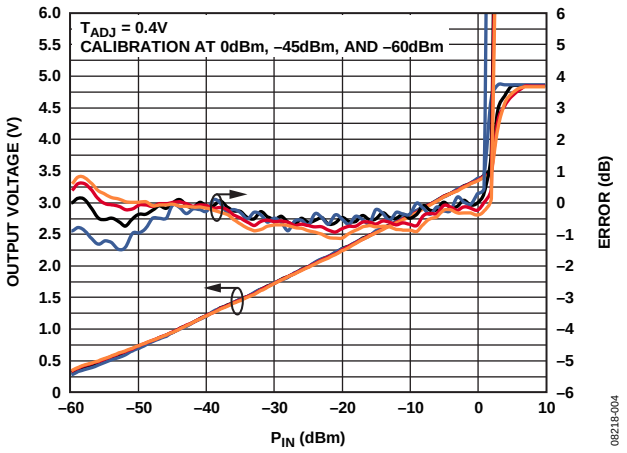

Figure 4. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 700 MHz, CW

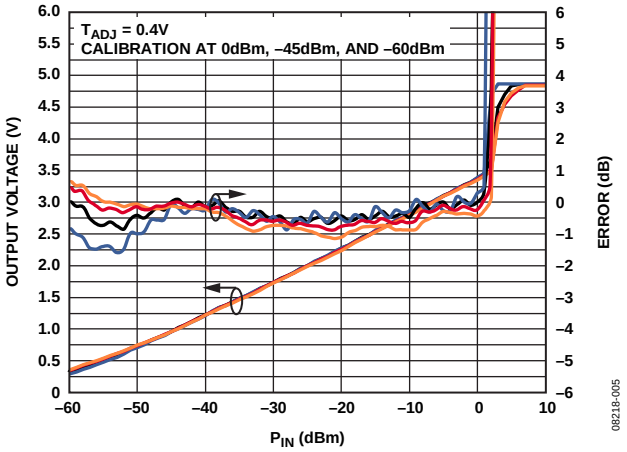

Figure 5. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 900 MHz, CW

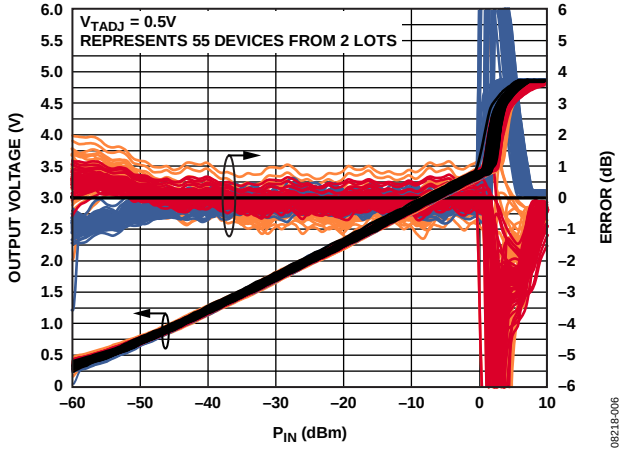

Figure 6. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 100 MHz

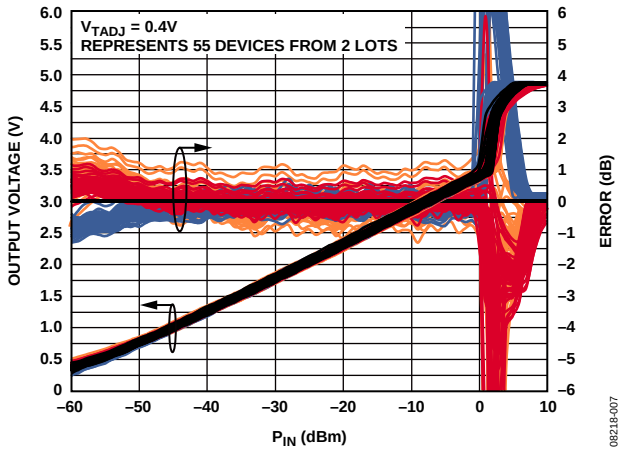

Figure 7. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 700 MHz

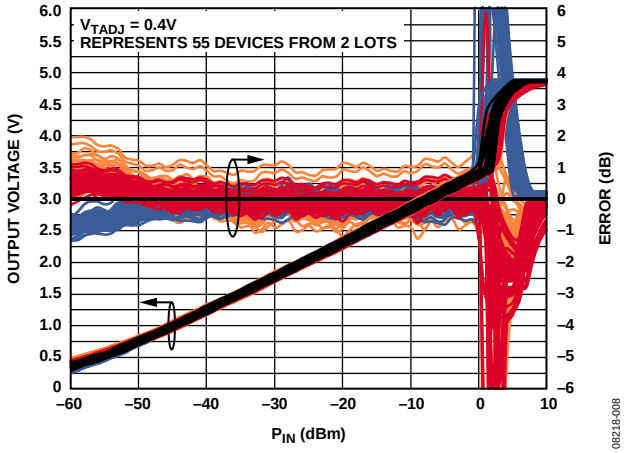

Figure 8. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 900 MHz

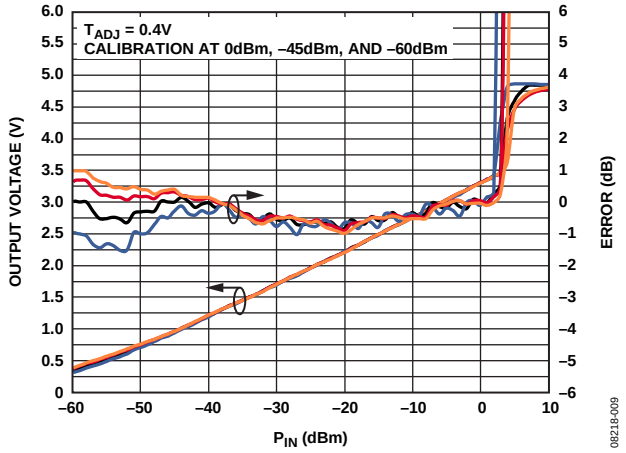

Figure 9. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 1.9 GHz, CW

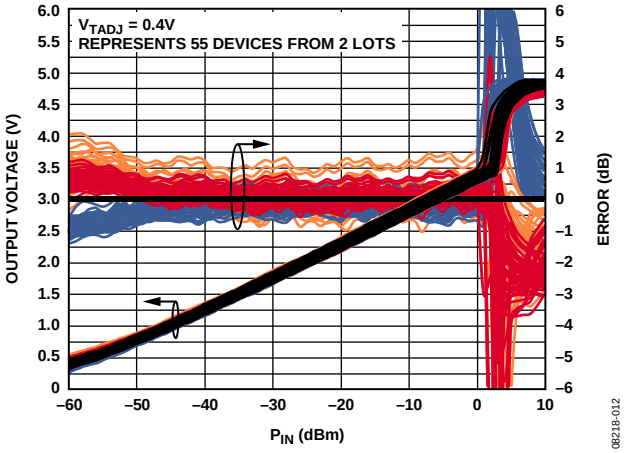

Figure 12. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 1.9 GHz

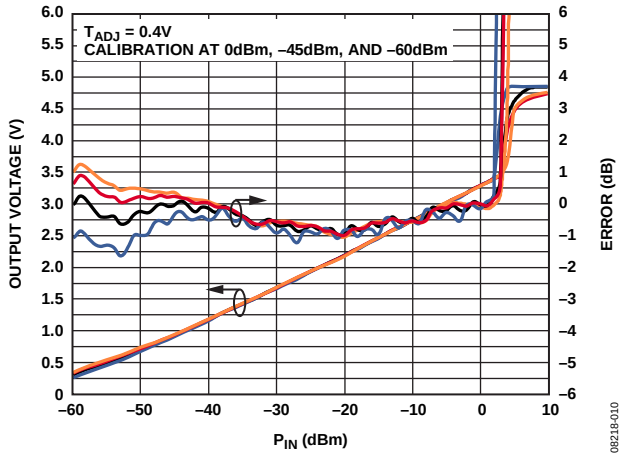

Figure 10. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.14 GHz, CW

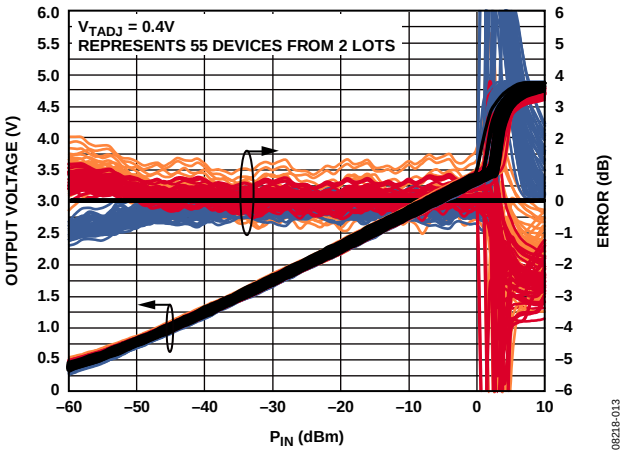

Figure 13. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 2.14 GHz

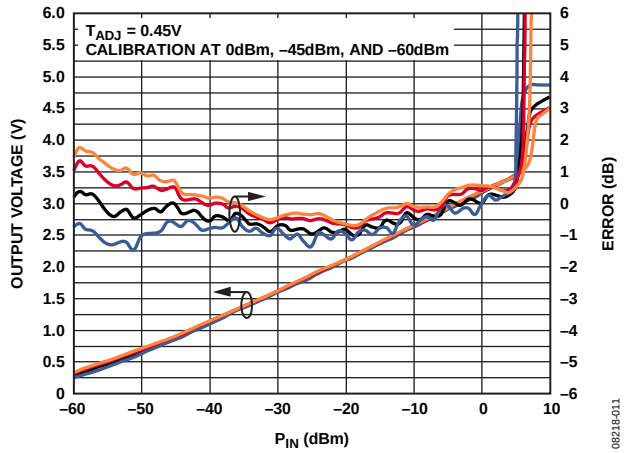

Figure 11. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.6 GHz, CW

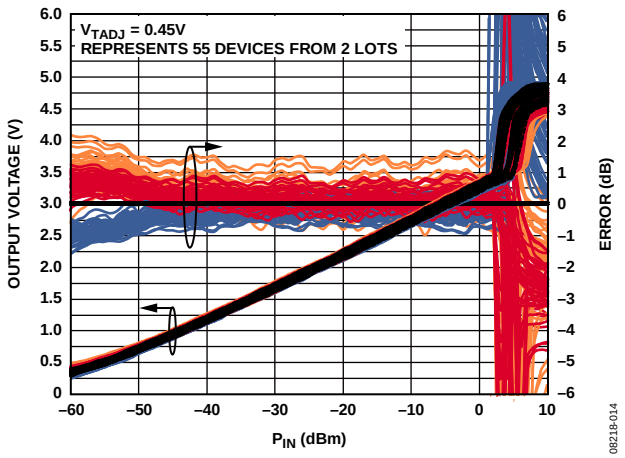

Figure 14. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 2.6 GHz

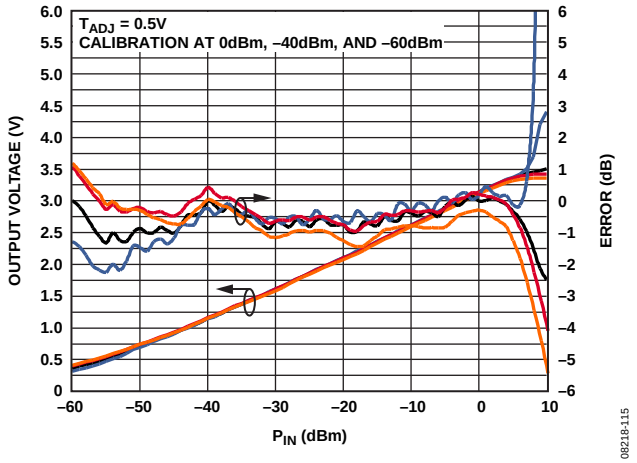

Figure 15. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 3.5 GHz, CW

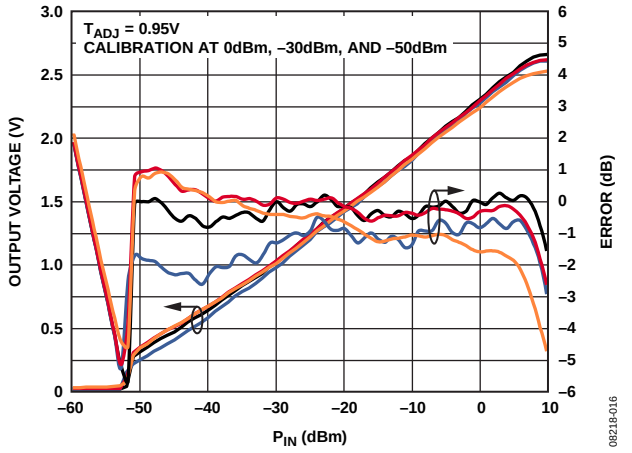

Figure 16. Typical V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 5.8 GHz, CW

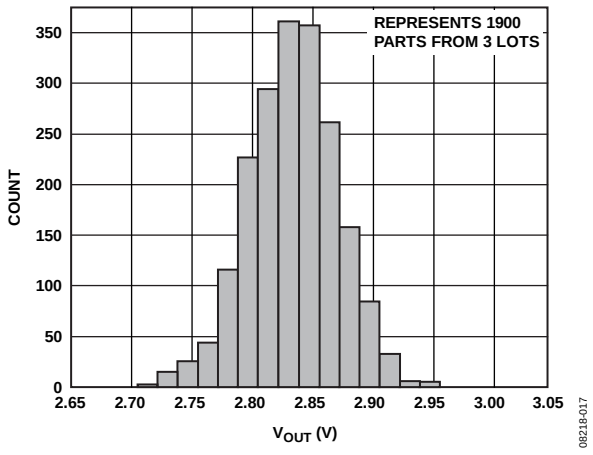

Figure 17. Distribution of V_{OUT}, P_{IN} = −10 dBm, 900 MHz

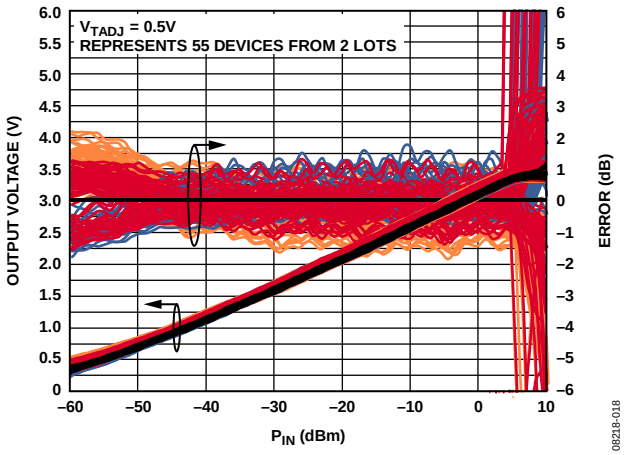

Figure 18. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 3.5 GHz

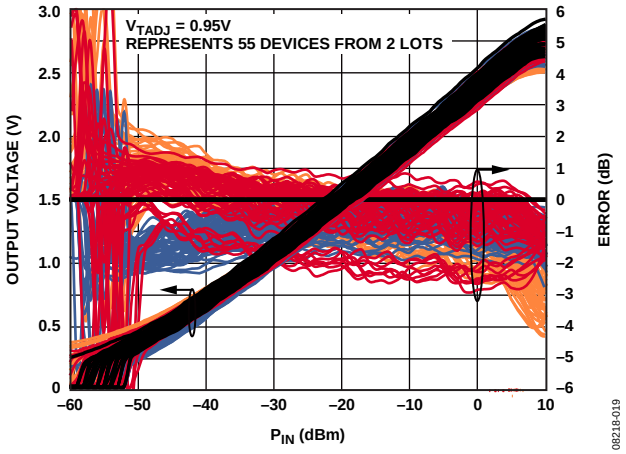

Figure 19. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude, CW, Frequency = 5.8 GHz

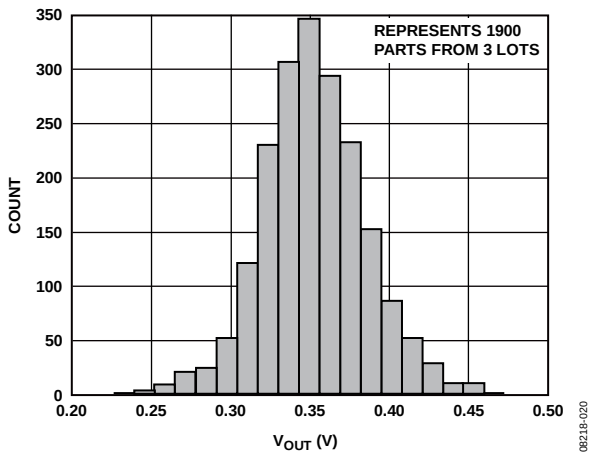

Figure 20. Distribution of V_{OUT}, P_{IN} = −60 dBm, 900 MHz

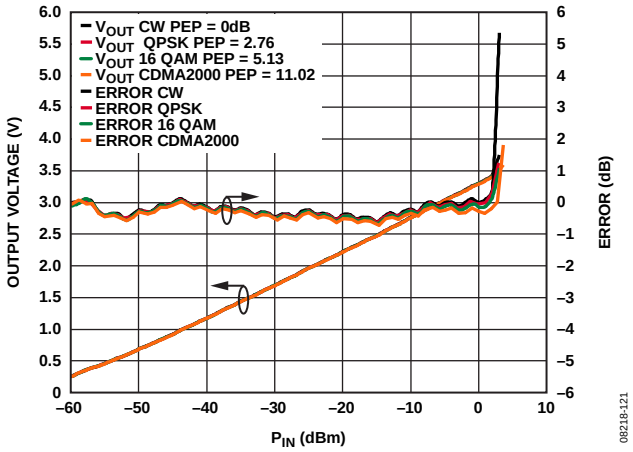

Figure 21. Error from CW Linear Reference vs. Signal Modulation, Frequency = 900 MHz, C_{LPF} = 0.1µF, Three-Point Calibration at 0 dBm, −45 dBm, and −60 dBm

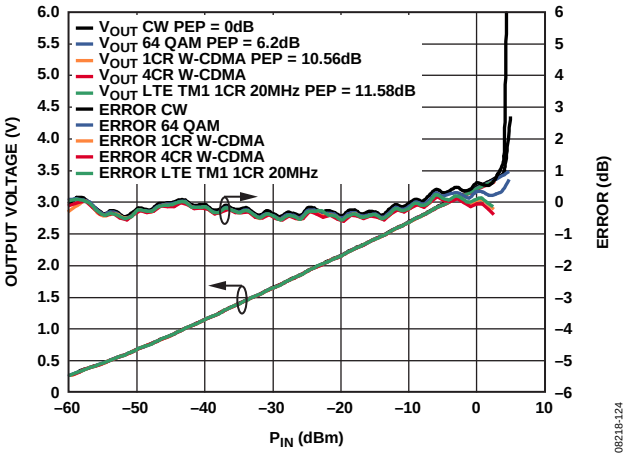

Figure 24. Error from CW Linear Reference vs. Signal Modulation, Frequency = 2.14 GHz, C_{LPF} = 0.1 µF, Three-Point Calibration at −10 dBm, −45 dBm, and −60 dBm

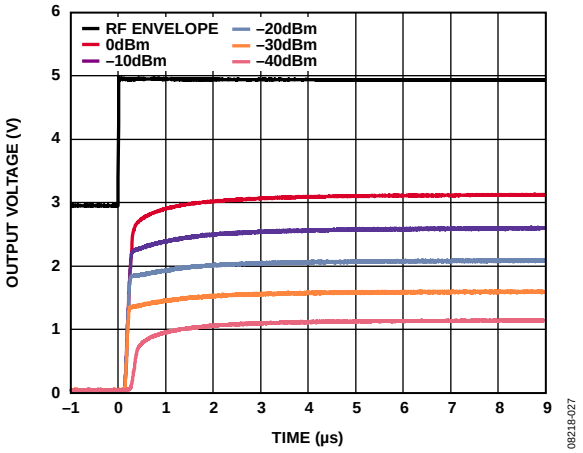

Figure 22. Output Response to RF Burst Input, Carrier Frequency 2.14 GHz, C_{LPF} = 220 pF, Rising Edge

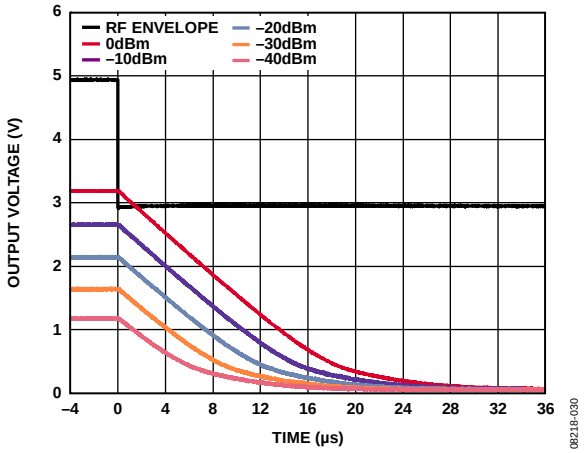

Figure 25. Output Response to RF Burst Input, Carrier Frequency 2.14 GHz, C_{LPF} = 220 pF, Falling Edge

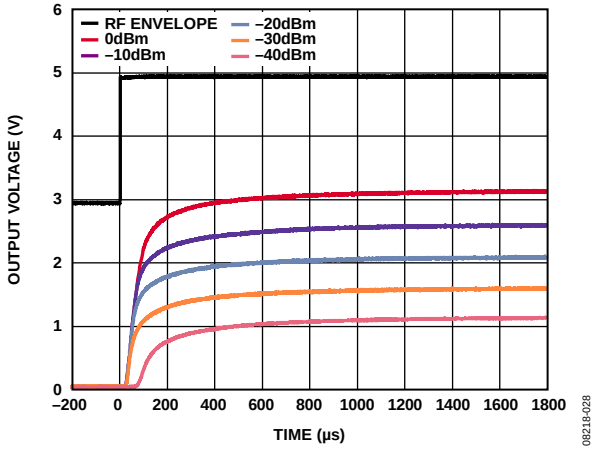

Figure 23. Output Response to RF Burst Input, Carrier Frequency 2.14 GHz, C_{LPF} = 0.1 µF, Rising Edge

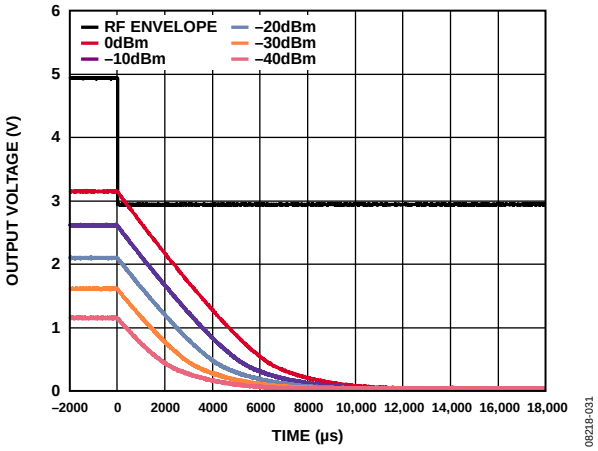

Figure 26. Output Response to RF Burst Input, Carrier Frequency 2.14 GHz, C_{LPF} = 0.1 µF, Falling Edge

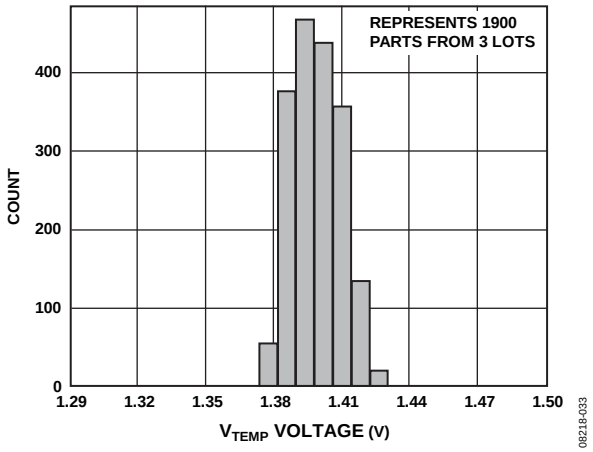

Figure 27. Distribution of V_{TEMP} Voltage at 25°C, No RF Input

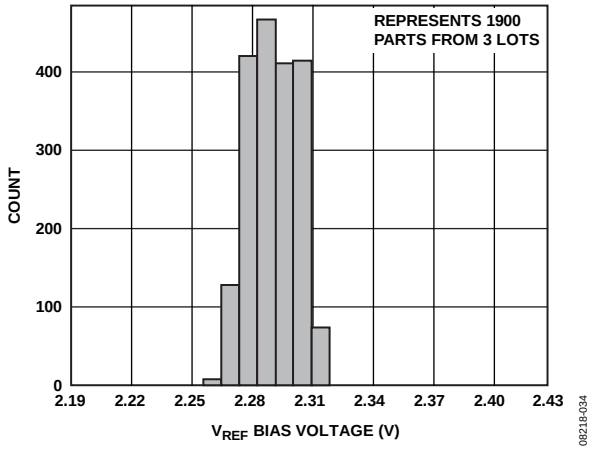

Figure 28. Distribution of V_{REF} Voltage at 25°C, No RF Input

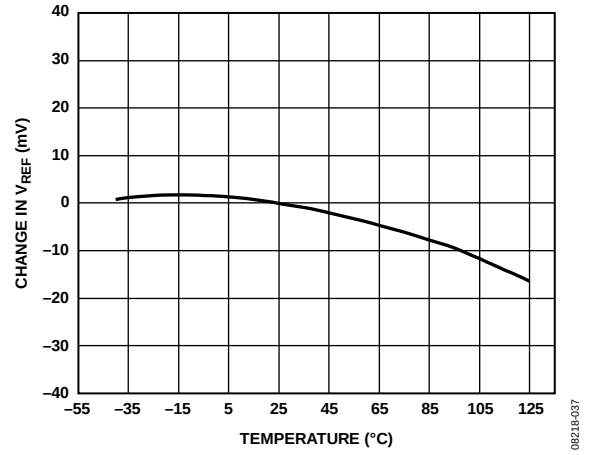

Figure 29. Change in V_{REF} vs. Temperature with Respect to 25°C, RF Input = −40 dBm, Typical Device

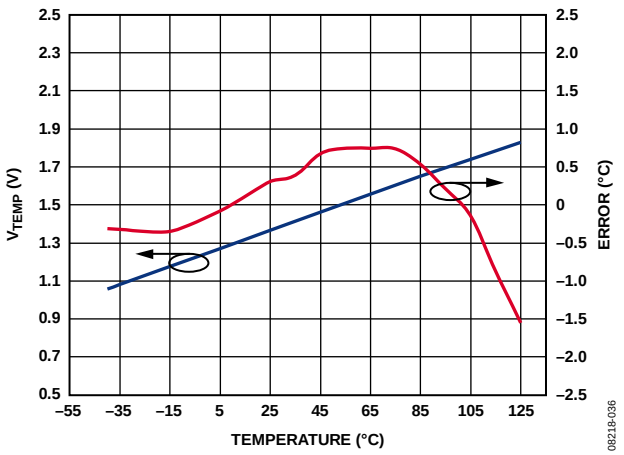

Figure 30. V_{TEMP} and Linearity Error with Respect to Straight Line vs. Temperature for Typical Device

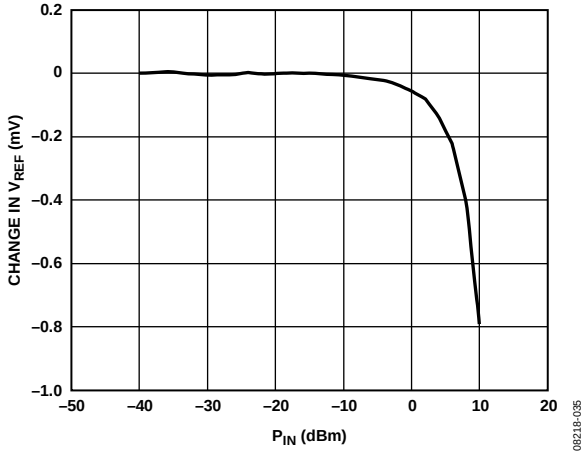

Figure 31. Change in V_{REF} vs. Input Amplitude with Respect to −40 dBm, 25°C, Typical Device

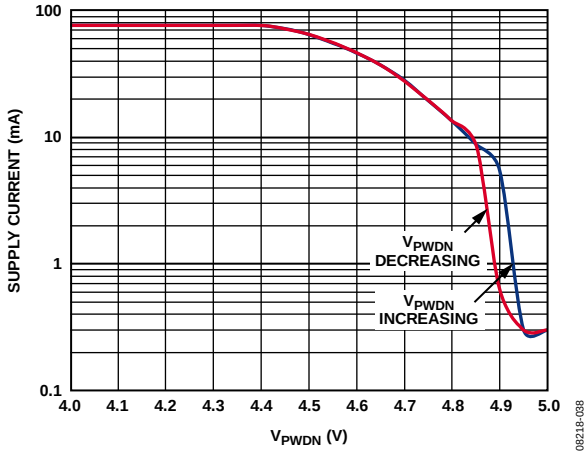

Figure 32. Supply Current vs. V_{PWDN}

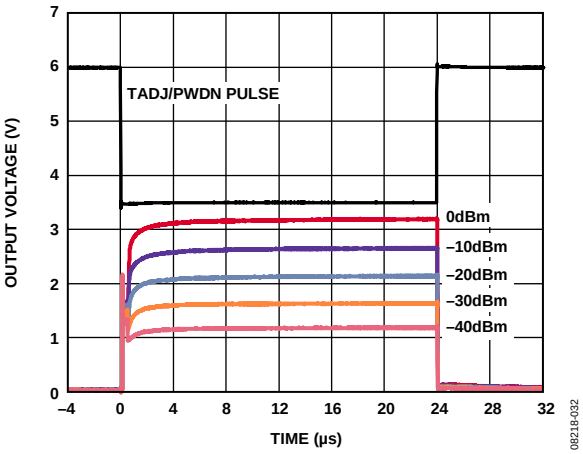

Figure 33. Output Response Using Power-Down Mode for Various RF Input Levels Carrier Frequency 2.14 GHz, C_{LPF} = 220 pF

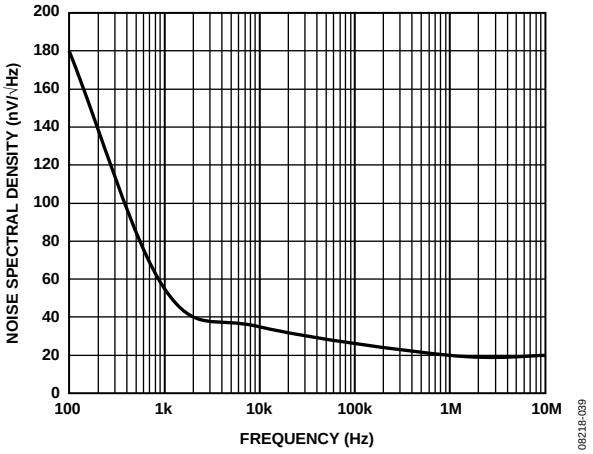

Figure 35. Noise Spectral Density of V_{OUT}, RF Input = –20 dBm, All C_{LPF} Values

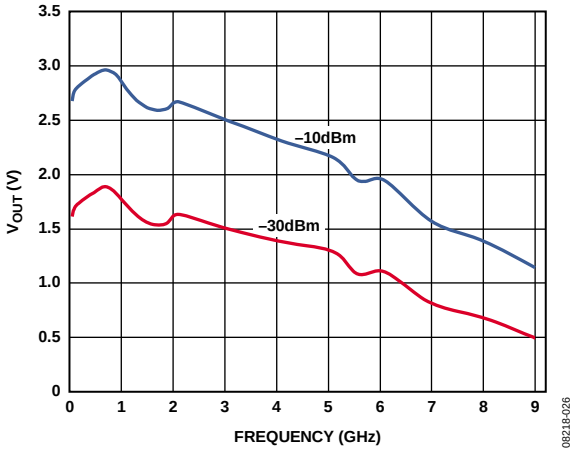

Figure 34. Typical V_{OUT} vs. Frequency for Two RF Input Amplitudes, 50 MHz to 9 GHz

THEORY OF OPERATION

The ADL5902 is a 50 MHz to 9 GHz true rms responding detector with a 65 dB measurement range at 2.14 GHz and a greater than 56 dB measurement range at frequencies up to 6 GHz. It incorporates a modified AD8362 architecture that increases the frequency range and improves measurement accuracy at high frequencies. Transfer function peak-to-peak ripple has been reduced to <±0.1 dB over the entire dynamic range. Temperature stability of the rms output measurements provides <±0.3 dB error, typically, over the specified temperature range of −40°C to 125°C through proprietary techniques. The device accurately measures waveforms that have a high peak-to-rms ratio (crest factor).

The ADL5902 consists of a high performance AGC loop. As shown in Figure 36, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver. For a more detailed description of the functional blocks, see the AD8362 data sheet.

The nomenclature used in this data sheet to distinguish between a pin name and the signal on that pin is as follows:

- The pin name is all uppercase, for example, VPOS, COMM, and VOUT.
- The signal name or a value associated with that pin is the pin mnemonic with a partial subscript, for example, C_{LPF} and V_{OUT}.

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The VGA gain has the form

$$G_{SET} = G_O \, e^{-(V_{SET}/V_{GNS})} \quad (1)$$

where:

G_O is the basic fixed gain.

V_{GNS} is a scaling voltage that defines the gain slope (the decibel change per voltage). The gain decreases with increasing V_{SET}.

The VGA output is

$$V_{SIG} = G_{SET} \times RF_{IN} = G_O \times RF_{IN} \, e^{-(V_{SET}/V_{GNS})} \quad (2)$$

where RF_{IN} is the ac voltage applied to the input terminals of the ADL5902.

The output of the VGA, V_{SIG}, is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform. The detector output, I_{SQR}, is a fluctuating current with positive mean value. The difference between I_{SQR} and an internally generated current, I_{TGT}, is integrated by the parallel combination of C_F and the external capacitor attached to the CLPF pin at the summing node. C_F is an on-chip 26 pF filter capacitor, and C_{LPF}, the external capacitance connected to the CLPF pin, can be used to arbitrarily increase the averaging time while trading off with the response time. When the AGC loop is at equilibrium

$$Mean(I_{SQR}) = I_{TGT} \quad (3)$$

This equilibrium occurs only when

$$Mean(V_{SIG}^2) = V_{TGT}^2 \quad (4)$$

where V_{TGT} is the voltage presented at the VTGT pin. This pin can conveniently be connected to the VREF pin through a voltage divider to establish a target rms voltage, V_{ATG}, of ~40 mV rms when V_{TGT} = 0.8 V.

Because the square law detectors are electrically identical and well matched, process and temperature dependent variations are effectively cancelled.

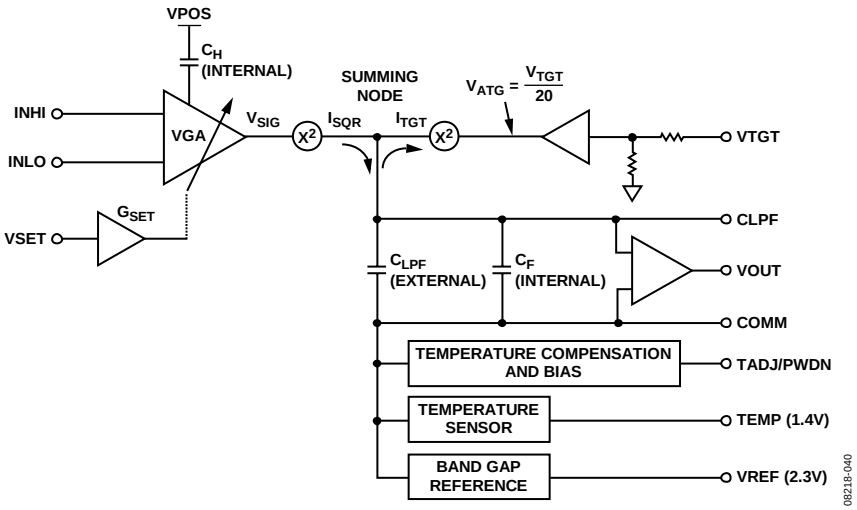

Figure 36. Simplified Architecture Details

When forcing the previous identity by varying the VGA setpoint, it is apparent that

$$RMS(V_{SIG}) = \sqrt{(Mean(V_{SIG}^2))} = \sqrt{(V_{ATG}^2)} = V_{ATG} \quad (5)$$

Substituting the value of V_{SIG} from Equation 2 results in

$$RMS(G_0 \times RF_{IN}\, e^{-(V_{SET}/V_{GNS})}) = V_{ATG} \quad (6)$$

When connected as a measurement device, $V_{SET} = V_{OUT}$. Solving for V_{OUT} as a function of RF_{IN},

$$V_{OUT} = V_{SLOPE} \times \log_{10}(RMS(RF_{IN})/V_Z) \quad (7)$$

where:
V_{SLOPE} is 1.06 V/decade (or 53 mV/dB) at 2.14 GHz.
V_Z is the intercept voltage.

When $RMS(RF_{IN}) = V_Z$, this implies that $V_{OUT} = 0$ V because $\log_{10}(1) = 0$. This makes the intercept the input that forces V_{OUT} = 0 V if the ADL5902 had no sensitivity limit. The $P_{INTERCEPT}$ (in decibels relative to 1 milliwatt, that is, dBm) corresponding to Vz (in volts) in ADL5902 is given by the following equation:

$$P_{INTERCEPT} = -(V_{PEDISTAL}/V_{SLOPE}) + P_{MINDET} \quad (8)$$

where $V_{PEDISTAL}$ is the VSET interface's pedestal voltage, and P_{MINDET} is the minimum detectable signal in decibels relative to 1 milliwatt, given by the following expression:

$$P_{MINDET} = dBm\,(V_{ATG}) - G_O \quad (9)$$

where $dBm(V_{ATG})$ is the equivalent power in decibels relative to 1 milliwatt corresponding to a given V_{TGT}.

Combining Equation 8 and Equation 9 results in

$$P_{INTERCEPT} = -(V_{PEDISTAL}/V_{SLOPE}) + dBm\,(V_{ATG}) - G_O \quad (10)$$

For the ADL5902, $V_{PEDISTAL}$ is approximately 0.275 V and V_{ATG} is given by $V_{TGT}/20$. G_O is 45 dB below approximately 4 GHz and then decreases at higher frequencies. V_{TGT} = 0.8 V; therefore,

$$V_{ATG} = 40 \text{ mV}$$

and

$$dBm\,(V_{ATG}) = 10 \log_{10}((40 \text{ mV})^2/50\ \Omega)/1 \text{ mW}) \approx -14.9 \text{ dBm}$$

At 2.14 GHz, $V_{SLOPE} \approx 53$ mV/dB and G_O at 2.14 GHz = 45 dB. This results in a $P_{INTERCEPT} \approx -65$ dBm. This differs slightly from the value in Table 1 due to the choice of calibration points and the slight nonideality of the response.

In most applications, the AGC loop is closed through the setpoint interface and the VSET pin. In measurement mode, VOUT is directly connected to VSET (see the Measurement Mode Basic Connections section for more information). In controller mode, a control voltage is applied to VSET, and the VOUT pin typically drives the control input of an amplification or attenuation system. In this case, the voltage at the VSET pin forces a signal amplitude at the RF inputs of the ADL5902 that balances the system through feedback.

RF INPUT INTERFACE

Figure 37 shows the RF input connections within the ADL5902. The input impedance is set primarily by an internal 2 kΩ resistor connected between INHI and INLO. A dc level of approximately half the supply voltage on each pin is established internally. Either the INHI or INLO pin can be used as the single-ended RF input pin. Signal coupling capacitors must be connected from the input signal to the INHI and INLO pins. A single external 60.4 Ω resistor to ground from the desired input creates an equivalent 50 Ω impedance over a broad section of the operating frequency range. The other input pin should be RF ac-coupled to common (ground). The input signal high-pass corner formed by the input coupling capacitor's internal and external resistances is

$$f_{HIGHPASS} = 1/(2 \times \pi \times 50 \times C) \quad (11)$$

where C is the capacitance in farads and $f_{HIGHPASS}$ is in hertz. The input coupling capacitors must be large enough in value to pass the input signal frequency of interest and determine the low end of the frequency response. INHI and INLO can also be driven differentially using a balun.

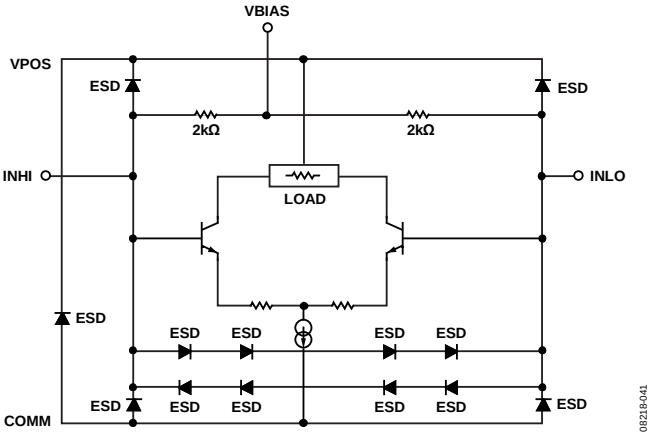

Figure 37. RF Inputs

Extensive ESD protection is employed on the RF inputs, and this protection limits the maximum possible input to the ADL5902.

SMALL SIGNAL LOOP RESPONSE

The ADL5902 uses a VGA in a loop to force a squared RF signal to be equal to a squared dc voltage. This nonlinear loop can be simplified and solved for a small signal loop response. The low-pass corner pole is given by

$$Freq_{LP} \approx 1.83 \times I_{TGT}/(C_{LPF}) \quad (12)$$

where:
I_{TGT} is in amperes.
C_{LPF} is in farads.
$Freq_{LP}$ is in hertz.

I_{TGT} is derived from V_{TGT}; however, I_{TGT} is a squared value of V_{TGT} multiplied by a transresistance, namely

$$I_{TGT} = g_m \times V_{TGT}^2 \quad (13)$$

g_m is approximately 18.9 µs; therefore, with V_{TGT} equal to the typically recommended 0.8 V, I_{TGT} is approximately 12 µA. The value of this current varies with temperature; therefore, the small signal pole varies with temperature. However, because the RF squaring circuit and dc squaring circuit track with temperature,

there is no temperature variation contribution to the absolute value of V_{OUT}.

For CW signals,

$$Freq_{LP} \approx 67.7 \times 10^{-6}/(C_{LPF}) \quad (14)$$

However, signals with large crest factors include low pseudo-random frequency content that must be either filtered out or sampled and averaged out (see the Choosing a Value for C_{LPF} section for more information).

TEMPERATURE SENSOR INTERFACE

The ADL5902 provides a temperature sensor output with a scaling factor of the output voltage of approximately 4.9 mV/°C. The output is capable of sourcing 4 mA and sinking 50 µA maximum at 25°C. An external resistor can be connected from TEMP to COMM to provide additional current sink capability. The typical output voltage at 25°C is approximately 1.4 V.

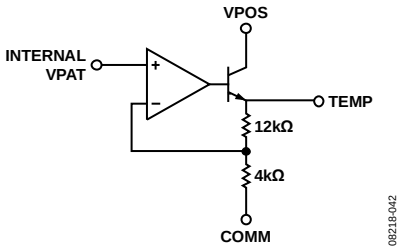

Figure 38. TEMP Interface Simplified Schematic

VREF INTERFACE

The VREF pin provides an internally generated voltage reference for the user. The VREF voltage is a temperature stable 2.3 V reference that is capable of sourcing 4 mA and sinking 50 µA maximum. An external resistor can be connected from VREF to COMM to provide additional current sink capability. The voltage on this pin can be used to drive the TADJ/PWDN and VTGT pins.

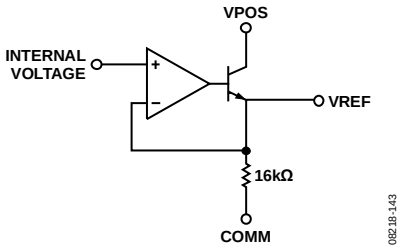

Figure 39. VREF Interface Simplified Schematic

TEMPERATURE COMPENSATION INTERFACE

While the ADL5902 has a highly stable measurement output with respect to temperature using proprietary techniques, for optimal performance, the output temperature drift must be compensated for using the TADJ pin. The absolute value of compensation varies with frequency and V_{TGT}. Table 4 shows the recommended voltages for V_{TADJ} to maintain a temperature drift error of typically ±0.5 dB or better over the intended temperature range (−40°C < T_A < +85°C) when driven single-ended and V_{TGT} = 0.8 V.

Table 4. Recommended V_{TADJ} for Selected Frequencies

Frequency	V_{TADJ} (V)	**R9 in** Figure 54 (Ω)	**R12 in** Figure 54 (Ω)
100 MHz	0.5	1430	402
700 MHz	0.4	1430	301
900 MHz	0.4	1430	301
1.9 GHz	0.4	1430	301
2.14 GHz	0.4	1430	301
2.6 GHz	0.45	1430	348
3.5 GHz	0.5	1430	402
5.8 GHz	0.95	1430	1007

The values in Table 4 were chosen to give the best drift performance at the high end of the usable dynamic range over the −40°C to +85°C temperature range. There is often a trade off in setting values, and optimizing for one area of the dynamic range may mean less than optimal drift performance at other input amplitudes.

Compensating the device for temperature drift using TADJ allows for great flexibility. If the user requires minimum temperature drift at a given input power, a subset of the dynamic range, or even over a different temperature range than shown in this data sheet, the V_{TADJ} can be swept while monitoring V_{OUT} over the temperature at the frequency and amplitude of interest. The optimal V_{TADJ} to achieve minimum temperature drift at a given power and frequency is the value of V_{TADJ} where the output has minimum movement.

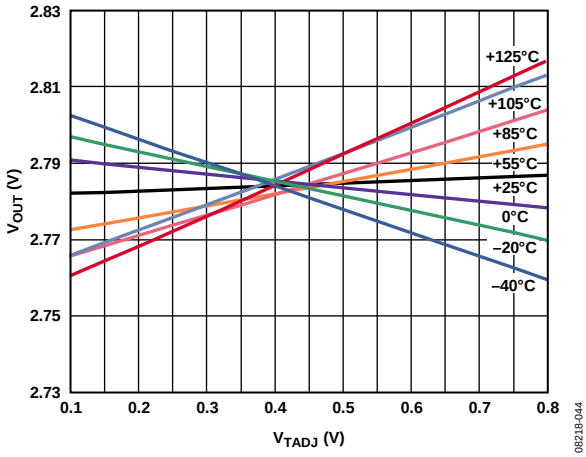

Figure 40. Effect of V_{TADJ} at Various Temperatures, 2.14 GHz, −10 dBm

Varying V_{TADJ} has only a very slight effect on V_{OUT} at device temperatures near 25°C; however, the compensation circuit has more and more effect as the temperature departs farther from 25°C.

The TADJ pin has a high input impedance and can be conveniently driven from an external source or from an attenuated value of V_{REF} using a resistor divider. Table 4 gives suggested voltage divider values to generate the required voltage from V_{REF}. The resistors are shown in the evaluation board schematic (see Figure 54). V_{REF} does change slightly with temperature and also input RF amplitude; however, the amount of change is unlikely to result in a significant effect on the final temperature

stability of the RF measurement system. Typically, the temperature compensation circuit responds only to voltages between 0 and $V_S/2$, or about 2.5 V when V_S = 5 V.

Figure 41 in the Power-Down Interface section shows a simplified schematic representation of the TADJ/PWDN interface.

POWER-DOWN INTERFACE

The quiescent and disabled currents for the ADL5902 at 25°C are approximately 73 mA and 300 µA, respectively. The dual function TADJ/PWDN pin is connected to the temperature compensation circuit as well as the power-down circuit. Typically, the temperature compensation circuit responds only to voltages between 0 and $V_S/2$, or about 2.5 V when V_S = 5 V.

When the voltage on this pin is greater than V_S – 0.1 V, the device is fully powered down. Figure 32 shows this characteristic as a function of V_{PWDN}. Note that, because of the design of this section of the ADL5902, as V_{PWDN} passes through a narrow range at ~4.5 V (or ~V_S – 0.5 V), the TADJ/PWDN pin sinks approximately 500 µA. The source used to disable the ADL5902 must have a sufficiently high current capability for this reason. Figure 33 shows the typical response times for various RF input levels. The output reaches within 0.1 dB of its steady-state value in approximately 5 µs; however, the reference voltage is available to full accuracy in a much shorter time. This wake-up response varies depending on the input coupling and C_{LPF}.

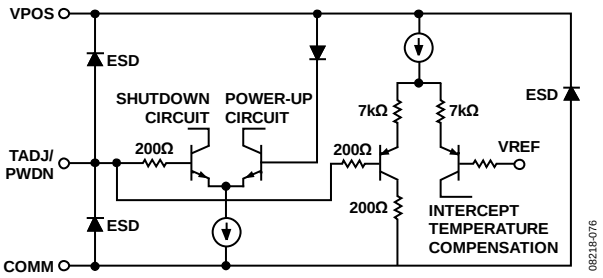

Figure 41. TADJ/PWDN Interface Simplified Schematic

VSET INTERFACE

The VSET interface has a high input impedance of 72 kΩ. The voltage at VSET is converted to an internal current used to set the internal VGA gain. The VGA attenuation control is approximately 19 dB/V.

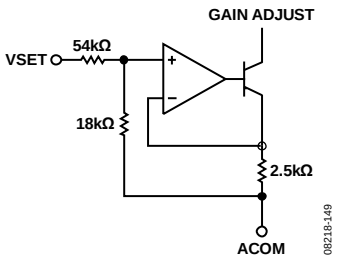

Figure 42. VSET Interface Simplified Schematic

OUTPUT INTERFACE

The ADL5902 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The closed-loop, – 3dB bandwidth from the input of the output amplifier to the output with no load is approximately 58 MHz with a single-pole roll off of approximately –20 dB/decade. The output noise is approximately 25 nV/√Hz at 100 kHz. The VOUT pin can source and sink up to 10 mA. There is also an internal load from VOUT to COMM of 2500 Ω.

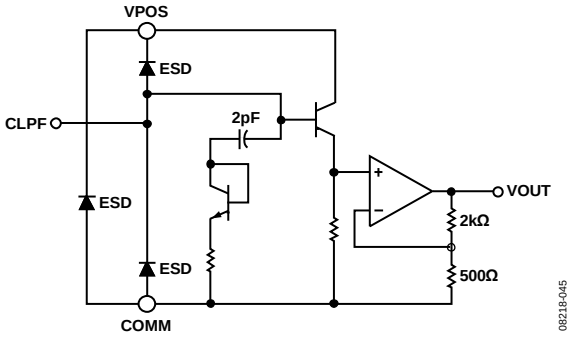

Figure 43. VOUT Interface Simplified Schematic

VTGT INTERFACE

The target voltage can be set with an external source or by connecting the VREF pin (nominally 2.3 V) to the VTGT pin through a resistive voltage divider. With 0.8 V on the VTGT pin, the rms voltage that must be provided by the VGA to balance the AGC feedback loop is 0.8 V × 0.05 = 40 mV rms. Most of the characterization information in this data sheet was collected at V_{TGT} = 0.8 V. Voltages higher and lower than this can be used; however, doing so increases or decreases the gain at the internal squaring cell, which results in a corresponding increase or decrease in intercept. This, in turn, affects the sensitivity and the usable measurement range, in addition to the sensitivity to different carrier modulation schemes. As V_{TGT} decreases, the squaring circuits produce more noise; this becomes noticeable in the output response at low input signal amplitudes. As V_{TGT} increases, measurement error due to modulation increases and temperature drift tends to decrease. The chosen V_{TGT} value of 0.8 V represents a compromise between these characteristics.

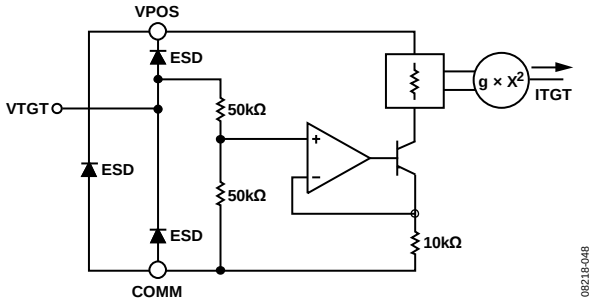

Figure 44. VTGT Interface

BASIS FOR ERROR CALCULATIONS

The slope and intercept used in the error plots are calculated using the coefficients of a linear regression performed on data collected in its central operating range. The error plots in the Typical Performance Characteristics section are shown in two formats: error from the ideal line and error with respect to the 25°C output voltage. The error from the ideal line is the decibel difference in V_{OUT} from the ideal straight-line fit of V_{OUT}

calculated by the linear-regression fit over the linear range of the detector, typically at 25°C. The error in decibels is calculated by

$$Error\ (dB) = (V_{OUT} - Slope \times (P_{IN} - P_Z))/Slope \quad (15)$$

where P_Z is the x-axis intercept expressed in decibels relative to 1 milliwatt (the input amplitude that would produce a 0 V output if such an output were possible).

The error from the ideal line is not a measure of absolute accuracy because it is calculated using the slope and intercept of each device. However, it verifies the linearity and the effect of temperature and modulation on the response of the device. An example of this type of plot is Figure 3. The slope and intercept that form the ideal line are those at 25°C with CW modulation. Figure 21 and Figure 24 show the error with various popular forms of modulation with respect to the ideal CW line. This method for calculating error is accurate, assuming that each device is calibrated at room temperature.

In the second plot format, the V_{OUT} voltage at a given input amplitude and temperature is subtracted from the corresponding V_{OUT} at 25°C and then divided by the 25°C slope to obtain an error in decibels. This type of plot does not provide any information on the linear-in-dB performance of the device; it merely shows the decibel equivalent of the deviation of V_{OUT} over temperature, given a calibration at 25°C. When calculating error from any one particular calibration point, this error format is accurate. It is accurate over the full range shown on the plot assuming that enough calibration points are used. Figure 6 shows this plot type.

The error calculations for Figure 30 are similar to those for the V_{OUT} plots. The slope and intercept of the V_{TEMP} function vs. temperature are determined and applied as follows:

$$Error\ (°C) = (V_{TEMP} - Slope \times (Temp - T_Z))/Slope \quad (16)$$

where:

T_Z is the x-axis intercept expressed in degrees Celsius (the temperature that would result in a V_{TEMP} of 0 V if this were possible).

Temp is the ambient temperature of the ADL5902 in degrees Celsius.

Slope is, typically, 4.9 mV/°C.

V_{TEMP} is the voltage at the TEMP pin at that temperature.

MEASUREMENT MODE BASIC CONNECTIONS

The ADL5902 requires a single supply of nominally 5 V. The supply is connected to the two VPOS supply pins. These pins should each be decoupled using the two capacitors with values equal or similar to those shown in Figure 45. These capacitors should be placed as close as possible to the VPOS pins.

An external 60.4 Ω resistor combines with the relatively high RF input impedance of the ADL5902 to provide a broadband 50 Ω match. An ac coupling capacitor should be placed between this resistor and INHI. The INLO input should be ac-coupled to ground using the same value capacitor. Because the ADL5902 has a minimum input operating frequency of 50 MHz, 100 pF ac coupling capacitors can be used.

The ADL5902 is placed in measurement mode by connecting VOUT to VSET. In measurement mode, the output voltage is proportional to the log of the rms input signal level.

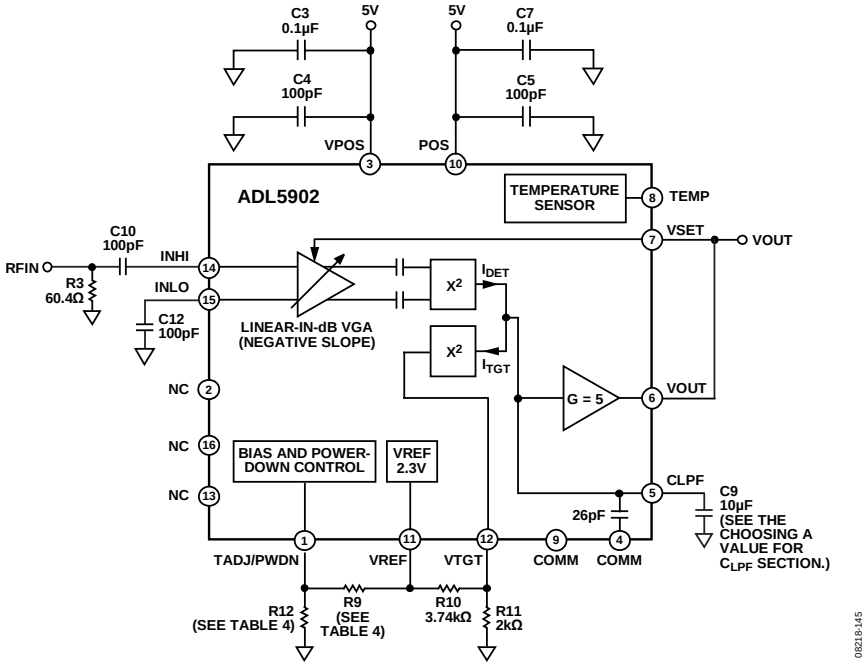

Figure 45. Basic Connections for Operation in Measurement Mode

SETTING V_{TADJ}

As discussed in the Theory of Operation section, the output temperature drift must be compensated by applying a voltage to the TADJ pin. The compensating voltage varies with frequency. The voltage for the TADJ pin can be easily derived from a resistor divider connected to the VREF pin. Table 5 shows the recommended V_{TADJ} for operation from −40°C to +85°C, along with resistor divider values. Resistor values are chosen so that they neither pull too much current from VREF (VREF short-circuit current is 4 mA) nor are so large that the TADJ pin's bias current of 3 µA affects the resulting voltage at the TADJ pin.

Table 5. Recommended V_{TADJ} for Selected Frequencies

Frequency	V_{TADJ} (V)	R9 (Ω)	R12 (Ω)
100 MHz	0.5	1430	402
700 MHz to 2.14 GHz	0.4	1430	301
2.6 GHz	0.45	1430	348
3.5 GHz	0.5	1430	402
5.8 GHz	0.95	1430	1007

SETTING V_{TGT}

As discussed in the Theory of Operation section, setting the voltage on VTGT to 0.8 V represents a compromise between achieving excellent rms compliance and maximizing dynamic range. The voltage on VTGT can be derived from the VREF pin using a resistor divider as shown Figure 45. Like the resistors chosen to set the V_{TADJ} voltage, the resistors setting V_{TGT} should have reasonable values that do not pull too much current from VREF or cause bias current errors. Also, attention should be paid to the combined current that VREF must deliver to generate the V_{TADJ} and V_{TGT} voltages. This current should be kept well below the VREF short-circuit current of 4 mA.

CHOOSING A VALUE FOR C_{LPF}

C_{LPF} provides the averaging function for the internal rms computation. Using the minimum value for C_{LPF} allows the quickest response time to a pulsed waveform but leaves significant output noise on the output voltage signal. By the same token, a large filter cap reduces output noise but at the expense of response time.

For non response-time critical applications, a relatively large capacitor can be placed on the CLPF pin. In Figure 45, a value of 10 µF is used. For most signal modulation schemes, this value ensures excellent rms measurement compliance and low residual output noise. There is no maximum capacitance limit for C_{LPF}.

Figure 46 shows how output noise varies with C_{LPF} when the ADL5902 is driven by a single-carrier W-CDMA signal (Test Model TM1-64, peak envelope power = 10.56 dB, bandwidth = 3.84 MHz). With a 10 µF capacitor on CLPF, there is residual noise on V_{OUT} of 4.4 mV p-p, which is less than 0.1 dB error (assuming a slope of approximately 53 mV/dB).

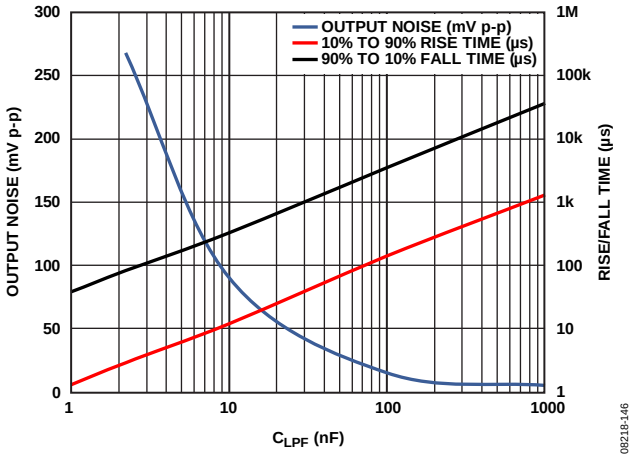

Figure 46. Output Noise, Rise and Fall Times vs. C_{LPF} Capacitance, Single-Carrier W-CDMA (TM1-64) at 2.14 GHz with P_{IN} = 0 dBm

Figure 46 also shows how the response time is affected by the value of C_{LPF}. To measure this, a RF burst at 2.14 GHz at −10 dBm was applied to the ADL5902. The 10% to 90% rise time and 90% to 10% fall time were then measured. It is notable that the fall time is much longer than the rise time. This can also be seen in the response time plots, Figure 22, Figure 23, Figure 25, and Figure 26.

In applications where the response time is critical, a different approach to signal filtering can be taken. This is shown in Figure 47. The capacitor on the CLPF pin is set to the minimum value that ensures that a valid rms computation has been performed. The job of noise removal is then handed off to an RC filter on the VOUT pin. This approach ensures that there is enough averaging to ensure good rms compliance and does not burden the rms computation loop with extra filtering that will significantly slow down the response time. By finishing the filtering process using an RC filter after VOUT, faster fall times can be achieved with an equivalent amount of output noise. It should be noted that the RC filter can also be implemented in the digital domain after the analog-to-digital converter.

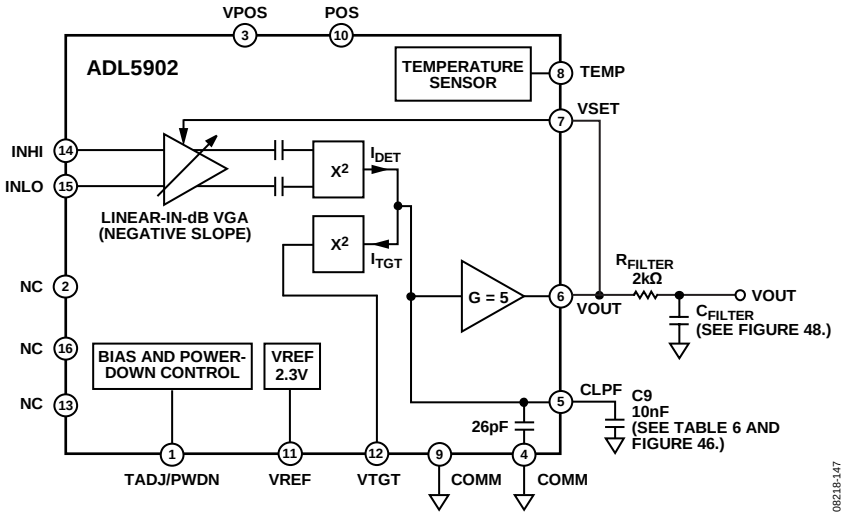

Figure 47. Optimizing Setting Time and Residual Ripple

In Figure 47, C_{LPF} is equal to 10 nF. This value was experimentally determined to be the minimum capacitance that ensures good rms compliance when the ADL5902 is driven by a 1 C W-CDMA signal (TM1-64). This test was carried out by starting out with a large capacitance value on the CLPF pin (for example, 10 µF). The value of V_{OUT} was noted for a fixed input power level (for example, −10 dBm). The value of C_{LPF} was then progressively reduced (this can be done with press-down capacitors) until the value of V_{OUT} started to deviate from its original value (this indicates that the accuracy of the rms computation is degrading and that C_{LPF} is getting too small).

Figure 48 shows the resulting rise and fall times (signal is pulsed between off and −10 dBm) with C_{LPF} equal to 10 nF. A 2 kΩ resistor is placed in series with the VOUT pin, and the capacitance from this resistor to ground (C_{FILTER} in Figure 47) is varied up to 1 µF.

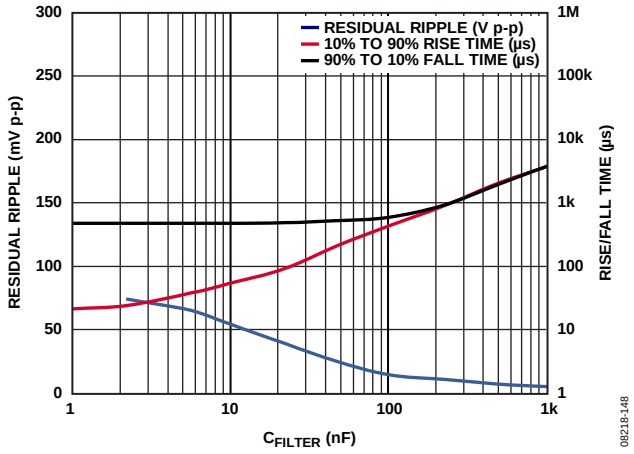

Figure 48. Residual Ripple, Rise and Fall Times Using an RC Low-Pass Filter at VOUT, P_{IN} = 0 dBm at 2.14 GHz

For large values of C_{FILTER}, the fall time is dramatically reduced compared to Figure 46. This comes at the expense of a moderate increase in rise time.

As C_{FILTER} is reduced, the fall time flattens out. This is because the fall time is now dominated by the 10 nF C_{LPF} which is present throughout the measurement.

Table 6 shows recommended minimum values of C_{LPF} for popular modulation schemes, using just a single filter capacitor at the CLPF pin. Using lower capacitor values results in rms measurement errors. Output response time (10% to 90%) is also shown. If the output noise shown in Table 6 is unacceptably high, it can be reduced by

- Increasing C_{LPF}
- Adding an RC filter at VOUT, as shown in Figure 47
- Implementing an averaging algorithm after the ADL5902's output voltage has been digitized by an ADC

Table 6. Recommended Minimum C_{LPF} Values for Various Modulation Schemes

Modulation/Standard	Peak-Envelope Power	Signal Bandwidth	C_{LPF} (min)	Output Noise	Rise/Fall Time (10% to 90%)
W-CDMA, One-Carrier, TM1-64	10.56 dB	3.84 MHz	10 nF	95 mV p-p	12/330 μs
W-CDMA Four-Carrier, TM1-64, TM1-32, TM1-16, TM1-8	12.08 dB	18.84 MHz	5.6 nF	164 mV p-p	7/200 μs
LTE, TM1 1CR 20 MHz (2048 Subcarriers, QPSK Subcarrier Modulation)	11.58 dB	20 MHz	1000 pF	452 mV p-p	1.3/38 μs

OUTPUT VOLTAGE SCALING

The output voltage range of the ADL5902 (nominally 0.3 V to 3.5 V) can be easily increased or decreased. There are a number of situations where adjustment of the output scaling makes sense. For example, if the ADL5902 is driving an analog-to-digital converter (ADC) with a 0 V to 5 V input range, it makes sense to increase the detector's nominal maximum output voltage of 3.5 V so that it is closer to 5 V. This makes better use of the input range of the ADC and maximizes the resolution of the system in terms of bits/dB.

If only a part of the ADL5902's RF input power range is being used (for example, −10 dBm to −60 dBm), it may make sense to increase the scaling so that this reduced input range fits into the ADL5902's available output swing of 0 V to 4.8 V.

The output swing can also be reduced by simply adding a voltage divider on the output pin, as shown in Figure 49. Reducing the output scaling may be used when interfacing the ADL5902 to an ADC with a 0 V to 2.5 V input range.

The output voltage swing can be increased using a technique that is analogous to setting the gain of an op amp in non-inverting mode with the VSET pin being the equivalent of the inverting input of the op amp.

Connecting VOUT to VSET results in the nominal 0 V to 3.5 V swing and a slope of approximately 53 mV/dB (this varies slightly with frequency). Figure 49 and Table 7 show the configurations for increasing the slope, along with recommended standard resistor values for particular input ranges and output swings.

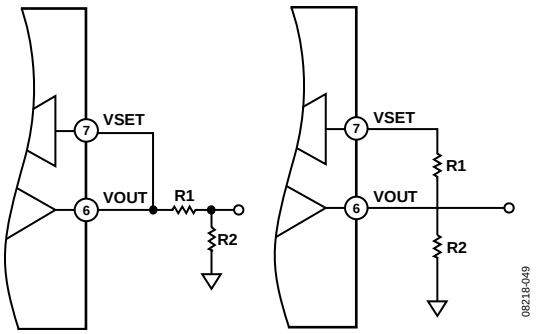

Figure 49. Decreasing and Increasing Slope

Table 7. Output Voltage Range Scaling

Desired Input Range (dBm)	R1 (Ω)	R2 (Ω)	New Slope (mV/dB)	Nominal Output Voltage Range (V)
0 to −60	665	2000	72.1	0.195 to 4.52
−10 to −50	1180	2000	86.3	1.096 to 4.55
0 to −60	806	2000	38.3	0.103 to 2.49
−10 to −50	324	2000	46.2	0.587 to 2.43

Equation 17 is the general function that governs this.

$$R1 = (R2 \parallel R_{IN})\left(\frac{V_O'}{V_O} - 1\right) \quad (17)$$

where:
V_O is the nominal maximum output voltage (see Figure 6 through Figure 18).
V'_O is the new maximum output voltage (for example, up to 4.8 V).
R_{IN} is the VSET input resistance (72 kΩ).

When choosing R1 and R2, attention must be paid to the current drive capability of the VOUT pin and the input resistance of the VSET pin. The choice of resistors should not result in excessive current draw out of VOUT. However, making R1 and R2 too large is also problematic. If the value of R2 is compatible with the input resistance of the VSET input (72 kΩ), this input resistance, which will vary slightly from part to part, contributes to the resulting slope and output voltage. In general, the value of R2 should be at least ten times smaller than the input resistance of VSET. Values for R1 and R2 should, therefore, be in the 1 kΩ to 5 kΩ range.

It is also important to take into account part-to-part and frequency variation in output swing along with the ADL5902 output stage's maximum output voltage of 4.8 V. The V_{OUT} distribution is well characterized at major frequencies' bands in the Typical Performance Characteristics section (see Figure 6 through Figure 8, Figure 12 through Figure 14, Figure 18, and Figure 19). The resistor values in Table 7, which were calculated based on 900 MHz performance, are conservatively chosen so that there is no chance that the output voltages exceed the ADL5902 output swing or the input range of a 0 V to 2.5 V and 0 V to 5 V ADC. Because the output swing does not vary much with frequency (it does start to drop off above 3 GHz), these values work for multiple frequencies.

SYSTEM CALIBRATION AND ERROR CALCULATION

The measured transfer function of the ADL5902 at 2.14 GHz is shown in Figure 50, which contains plots of both output voltage vs. input amplitude (power) and calculated error vs. input level. As the input level varies from −62 dBm to +3 dBm, the output voltage varies from ~0.25 V to ~3.5 V.

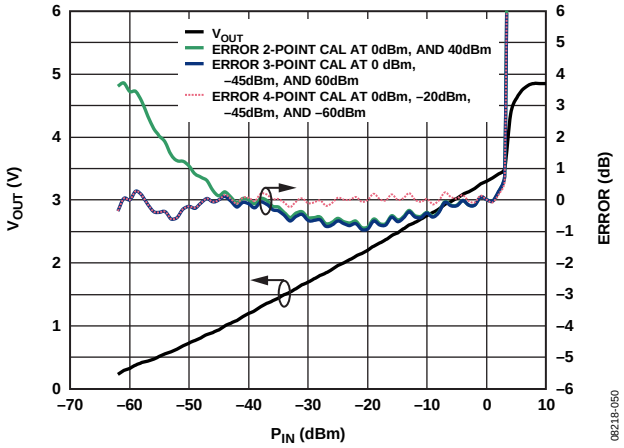

Figure 50. 2.14 GHz Transfer Function, Using Various Calibration Techniques

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. The equation for the idealized output voltage can be written as

$$V_{OUT(IDEAL)} = Slope \times (P_{IN} - Intercept) \quad (18)$$

where:
Slope is the change in output voltage divided by the change in input power (dB).
Intercept is the calculated input power level at which the output voltage is 0 V (note that *Intercept* is an extrapolated theoretical value not a measured value).

In general, calibration is performed during equipment manufacture by applying two or more known signal levels to the input of the ADL5902 and measuring the corresponding output voltages. The calibration points are generally within the linear-in-dB operating range of the device.

With a two-point calibration, the slope and intercept are calculated as follows:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2}) \quad (19)$$

$$Intercept = P_{IN1} - (V_{OUT1}/Slope) \quad (20)$$

After the slope and intercept are calculated and stored in nonvolatile memory during equipment calibration, an equation can be used to calculate an unknown input power based on the output voltage of the detector.

$$P_{IN}\,(Unknown) = (V_{OUT1(MEASURED)}/Slope) + Intercept \quad (21)$$

The log conformance error is the difference between this straight line and the actual performance of the detector.

$$Error\,(dB) = (V_{OUT(MEASURED)} - V_{OUT(IDEAL)})/Slope \quad (22)$$

Figure 50 includes a plot of this error when using a two-point calibration (calibration points are 0 dBm and −40 dBm). The error at the calibration points (in this case, −40 dBm and 0dBm) is equal to 0 by definition.

The residual nonlinearity of the transfer function that is apparent in the two-point calibration error plot can be reduced by increasing the number of calibration points. Figure 50 shows the postcalibration error plots for three-point and four-point calibrations. With a multipoint calibration, the transfer function is segmented, with each segment having its own slope and intercept. Multiple known power levels are applied, and multiple voltages are measured. When the equipment is in operation, the measured voltage from the detector is first used to determine which of the stored slope and intercept calibration coefficients are to be used. Then the unknown power level is calculated by inserting the appropriate slope and intercept into Equation 21.

Figure 51 shows the output voltage and error at 25°C and over temperature when a four-point calibration is used (calibration points are 0 dBm, −20 dBm, −45 dBm, and −60 dBm). When choosing calibration points, there is no requirement for, or value, in equal spacing between the points. There is also no limit to the number of calibration points used. However, using more calibration points increases calibration time.

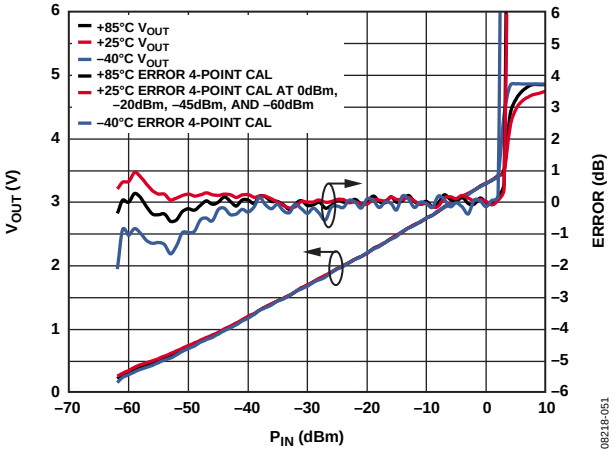

Figure 51. 2.14 GHz Transfer Function and Error at +25°C, −40°C, and +85°C Using a Four-Point Calibration (0 dBm, −20 dBm, −45 dBm, −60 dBm)

The −40°C and +85°C error plots in Figure 51 are generated using the 25°C calibration coefficients. This is consistent with equipment calibration in a mass production environment where calibration at just a single temperature is practical.

HIGH FREQUENCY PERFORMANCE

The ADL5902 is specified to 6 GHz; however, operation is possible to as high as 9 GHz with sufficient dynamic range for many purposes. Figure 52 shows the typical V_{OUT} response and conformance error at 7 GHz, 8 GHz, and 9 GHz.

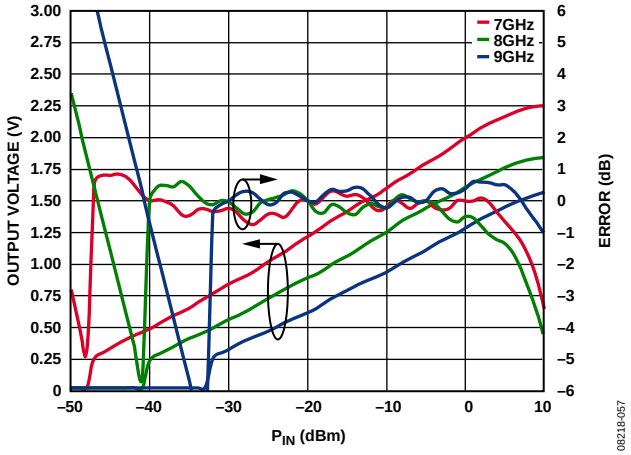

Figure 52. Typical V_{OUT} and Log Conformance Error at 7 GHz, 8 GHz, and 9 GHz, 25°C Only

LOW FREQUENCY PERFORMANCE

The lowest frequency of operation of the ADL5902 is approximately 50 MHz. This is the result of the circuit design and architecture of the ADL5902.

DESCRIPTION OF CHARACTERIZATION

The general hardware configuration used for most of the ADL5902 characterization is shown in Figure 53. The ADL5902 was driven in a single-ended configuration for most characterization, except where noted.

Much of the data was taken using an Agilent E4438C signal source as a RF input stimulus. Several ADL5902 devices mounted on circuit boards constructed of Rodgers 3006 material were put into a test chamber simultaneously, and a Keithley S46 RF switching network connected the signal source to the appropriate device under test. The test chamber temperature was set to cycle over the appropriate temperature range. The signal source, switching, and chamber temperature were all controlled by a PC running Agilent VEE Pro.

The subsequent response to stimulus was measured with a voltmeter and the results stored in a database for analysis later. In this way, multiple ADL5902 devices were characterized over amplitude, frequency, and temperature in a minimum amount of time. The RF stimulus amplitude was calibrated up to the circuit board that carries the ADL5902, and, thus, it does not account for the slight losses due to the connector on the circuit board that carries the ADL5902 nor for the loss of traces on the circuit board. For this reason, there is a small absolute amplitude error (generally <0.5 dB) not accounted for in the characterization data, but this is generally not important because the ADL5902's relative accuracy is unaffected.

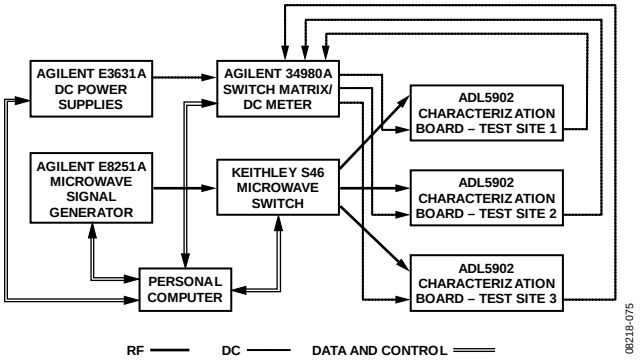

Figure 53. General Characterization Configuration

EVALUATION BOARD SCHEMATICS AND ARTWORK

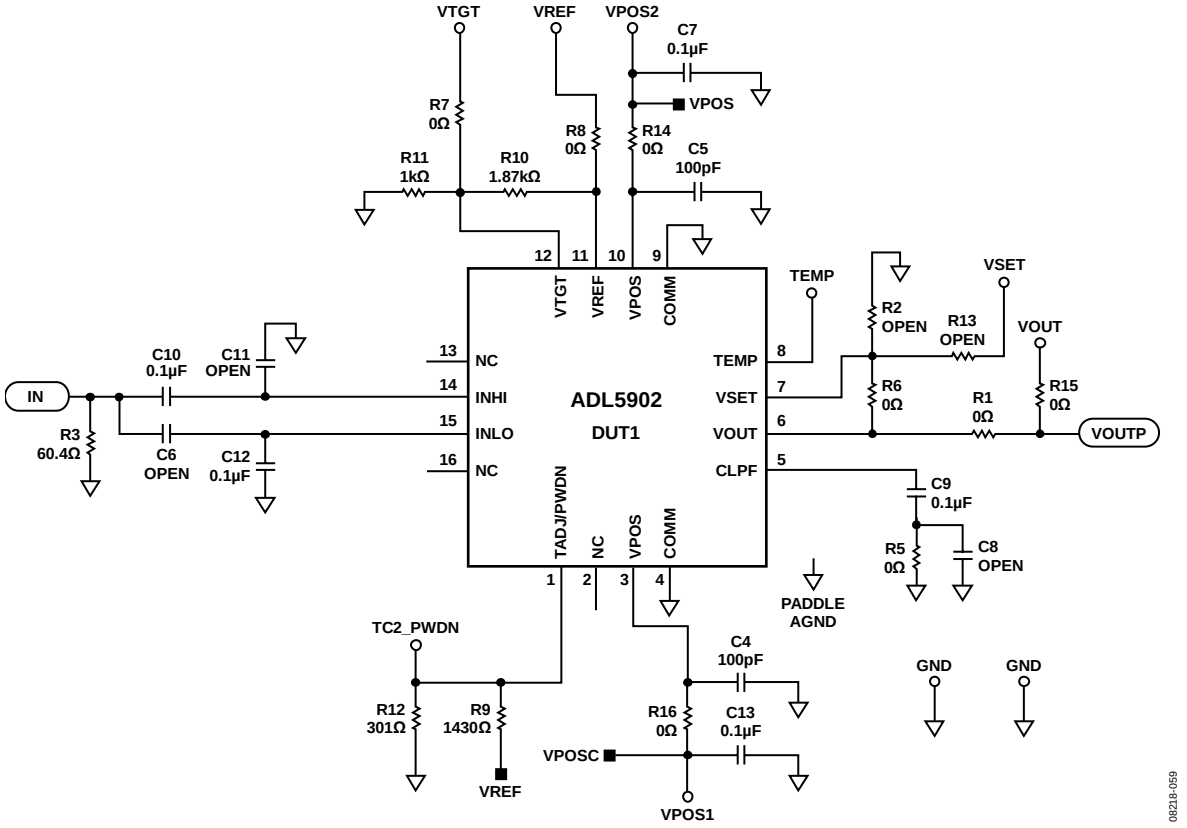

Figure 54. Evaluation Board Schematic

Table 8. Evaluation Board Configuration Options

Component	Function/Notes	Default Value
C6, C10, C11, C12, R3	RF input. The ADL5902 is generally driven single-ended. When driving INHI, populate C10 and C12 with an appropriate capacitor value for the frequency of operation and leave C6 and C11 open. When driving INLO, populate C6 and C11 with an appropriate capacitor value for the frequency of operation and leave C10 and C12 open. R3 is the input termination resistor and is chosen to give a 50 Ω input impedance over a broad frequency range.	C6 = open, C10 = C12 = 0.1 µF, C11 = open, R3 = 60.4 Ω
R7, R8, R10, R11	VTGT interface. R10 and R11 are set up to provide 0.8 V to VTGT derived from VREF. If R10 and R11 are removed, an external voltage can be applied. Alternatively, R7 and R11 can be used to form a voltage divider for an external reference.	R7 = R8 = 0 Ω, R10 = 1.87 kΩ, R11 = 1k Ω
C4, C5, C7, C13, R14, R16	Power supply decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed close to the ADL5902, a 0 Ω series resistor, and a 0.1 µF capacitor placed close to the power supply input pin.	C4 = C5 = 100 pF, C7 = C13 = 0.1 µF, R14 = R16 = 0 Ω
R1, R2, R6, R13, R15	Output interface. In measurement mode, a portion of the voltage at the VOUT pin is fed back to the VSET pin via R6. Using the voltage divider created by R2 and R6, the magnitude of the slope of V_{OUT} is increased by reducing the portion of V_{OUT} that is fed back to V_{SET}. In controller mode, R6 must be open and R13 must have a 0 Ω resistor. In this mode, the ADL5902 can control the gain of an external component. A setpoint voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the ADL5902.	R1 = R6 = R15 = 0 Ω, R2 = R13 = open
C8, C9, R5	Low-pass filter capacitors, C_{LPF}. The low-pass filter capacitors reduce the noise on the output and affect the response time of the ADL5902.	C8 = open, C9 = 0.1 µF, R5 = 0 Ω,
R9, R12	TADJ/PWDN. The TADJ/PWDN pin controls the amount of nonlinear intercept temperature compensation and/or shuts down the device. The evaluation board is configured with TADJ connected to VREF through a resistor divider (R9, R12).	R9 = 1430 Ω R12 = 301 Ω
Paddle	The paddle should be tied to both a thermal ground and an electrical ground.	

ASSEMBLY DRAWINGS

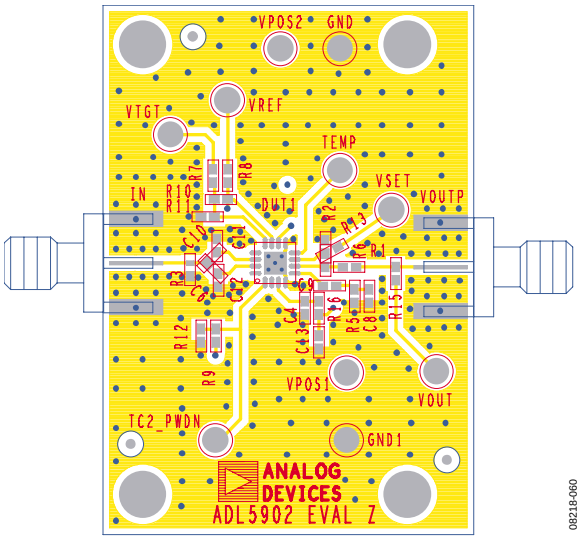

Figure 55. Evaluation Board Layout, Top Side

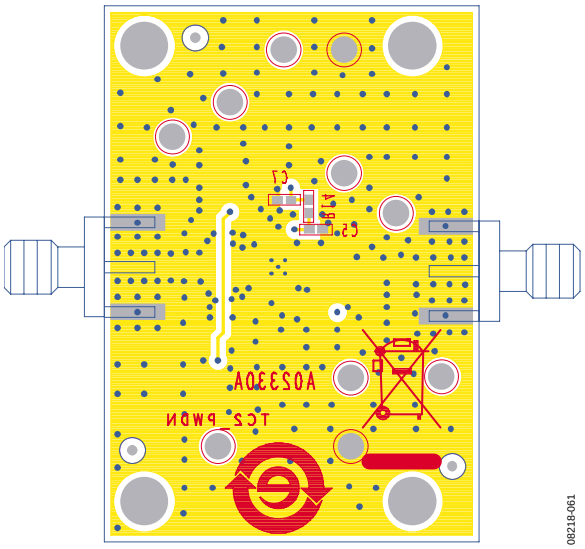

Figure 56. Evaluation Board Layout, Bottom Side

OUTLINE DIMENSIONS

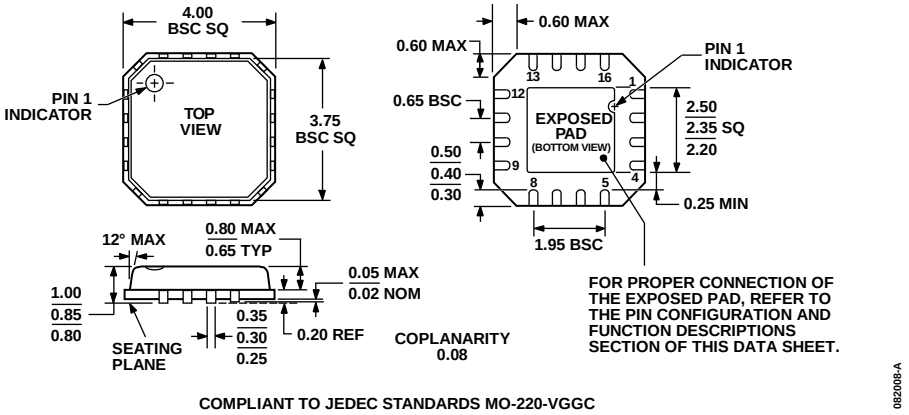

Figure 57. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5902ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	1,500
ADL5902ACPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	250
ADL5902ACPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	64
ADL5902-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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